

## CURRICULUM VITAE

### Personal Information

First Name: **XUAN TU**      Last name: **TRAN**      Sex: **Male**  
Date of Birth: 19 September 1977      Marital Status: Married, a daughter  
Place of Birth: Nghe An, Vietnam      Nationality: Vietnam  
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### Education

- From 01/2005 to 02/2008      Institut National Polytechnique de Grenoble (INPG), Grenoble, France  
**PhD in Micro Nano Electronics.**  
*Thesis:* Test Method and Design-for-Test of Asynchronous Networks-on-Chip: Application to ANOC network.  
*Keywords:* Design-for-Test, Network-on-Chip (NoC), System-on-Chip (SoC), Testability
- From 10/2000 to 10/2002      Vietnam National University, Hanoi.  
**Master of Science (MSc.) in Electronics and Communication.**      Grade: **Excellent**  
*Thesis:* “Design and Implementation of a System for Measuring and Transferring Data via Power-Line Networks”.  
*Keywords:* Power Line Communication (PLC), Micro-controller, Embedded system.
- From 09/1995 to 06/1999      Hanoi University of Science, Vietnam.  
**Bachelor of Science (BSc.) in Electronics and Communication.**      Grade: **Excellent**  
*Thesis:* “Design and Implementation of a General-Purpose Data Collection and Control System based on Micro-Controllers 8051”.
- From 09/1992 to 06/1995      Pupil of Huynh Thuc Khang high school, Vinh city, Nghe An province, Vietnam.  
**Baccalaureate**      Grade: **Good**

### Languages:

Vietnamese (native), English (fluently), French (good).

### Employments and work experiences

- From 12/1999 to present      **Lecturer (Assistant Professor)** of the University of Engineering and Technology (aka: College of Technology), Vietnam National University, Hanoi (UET-VNU). Head of VLSI Systems Design Laboratory from 12/2008, Vice-Director of Key Laboratory on Smart Integrated Systems (SIS Lab) from 04/2008.
- From 07/2009 to 08/2009      **Visiting professor** at the University of Paris-Sud 11 and the CEA-LETI, MINATEC.
- From 01/2005 to 02/2008      CEA-LETI, MINATEC – ASIC Department, Grenoble, France  
**R&D engineer**  
*Research Interests:* Design-for-Test (DfT), Network on Chip (NoC), System on Chip (SoC) testing, Testability, Asynchronous/synchronous VLSI design.
- From 07/2003 to 12/2004      CEA-LETI, MINATEC – ASIC Department, Grenoble, France  
**Internship**  
*Subject of internship:* “Design and implementation of a Viterbi decoder for the FAUST, a Flexible Architecture of Unified System for Telecom”.  
*Keywords:* Viterbi decoder, System on Chip (SoC), Network on Chip (NoC).

From 07/1999 to 11/1999 **Research engineer** at the Institute of Vietnam Electronics - Informatics and Automation (VIELINA), Ministry of Industries of Vietnam.

### Special skills in works

- Research interests: Design and Test of System-on-Chip, Network-on-Chip (NoC); Design-for-Test/Testability, Embedded System, Asynchronous/synchronous VLSI design.
- CAD/EDA tools: ModelSim, Leonardo Spectrum (Mentor Graphics); Virtuoso, PKS, SoC Encounter, Nanosim (Cadence); LEDA, VCS, Design Compiler (Synopsys).
- Programming languages: VHDL, SystemC, CHP, C++, Matlab, Assembler.
- Office tools: Linux, Unix, Windows Vista/XP/2000, MS office, LaTeX, Emacs, Vim.

### Professional activities

- Membership: IEEE (2006-), Radio-Electronics Association of Vietnam (2001-).
- TPC member, reviewer: IEEE-DELTA 2010, ATC 2009, ATC 2008, IEEE-ETS 2008, ICCE 2008, Journal of Information and Communication Technologies.

### Some Awards and Achievements

- 2008 Award from the UET-VNU for scientific research activities (2008).
- 2006 Scholarship from Rhône-Alpes region (2006-2007)
- 2005 Fellowship from the CEA-LETI (3 years from 2005 to 2008)
- 2003 Scholarship from the CEA-LETI for an internship (1 year ½ )
- 2002 Diploma of merit from the National Youth Association for social activities.
- 2001 Diploma of merit from Hanoi Youth Association for social activities.
- 1999 Awards of Association of Japanese Banks for the excellent results in study and research.
- 1999 Certificate of merit from Hanoi University of Science for the many achievements in study.
- 1998 The 2<sup>rd</sup> prize in the Scientific Research Contest for students at Hanoi University of Science
- 1997 Certificate of merit from Hanoi University of Science for the many achievements in study and social activities.

### Hobbies

- Badminton, ping-pong, jogging, ski, travel.
- Music, literatures.

## LIST OF PUBLICATIONS

1. Yvain Thonnart, Xuan-Tu Tran, Pascal Vivet, Edith Beigné, Fabien Clermidy, Jean Durupt. An Asynchronous Low-Power Innovative Network-on-Chip including Design-for-Test capabilities. In Proceedings of the **2009 International Conference on Advanced Technologies for Communications (ATC 2009)**, pp. 59–62, Hai Phong, Vietnam, October 2009. (Invited paper).
2. Xuan-Tu Tran, Yvain Thonnart, Jean Durupt, Vincent Beroulle, and Chantal Robach. Design-for-Test Approach of an Asynchronous Network-on-Chip Architecture and its Associated Test Pattern Generation and Application. **IET Journal on Computers and Digital Techniques**, Volume 3, Issue 5, pp. 487-500 (DOI:10.1049/iet-cdt.2008.0072) September 2009.
3. Beigne, E.; Clermidy, F.; Lhermet, H.; Miermont, S.; Thonnart, Y.; Tran, X.; Valentian, A.; Varreau, D.; Vivet, P.; Popon, X.; Lebreton, H. An Asynchronous Power Aware and Adaptive NoC Based Circuit. **IEEE Journal of Solid State Circuits (JSSC)**, Volume 44, Issue 4, pp. 1167-1177 (DOI: 10.1109/JSSC.2009.2014206), April 2009.
4. P.T. Hong, Phi-Hung Pham, Xuan-Tu Tran, Chulwoo Kim. Analysis and evaluation of traffic-performance in a backtracked routing network-on-chip. In Proceedings of the **2008 International Conference on Communications and Electronics (ICCE 2008)**, pp. 13–17, Hoi An, Vietnam, June 2008.
5. E. Beigne, F. Clermidy, J. Durupt, H. Lhermet, S. Miermont, Y. Thonnart, T. Tran-Xuan (X.-T. Tran), A. Valentian, D. Varreau, P. Vivet. An Asynchronous Power Aware and Adaptive NoC Based Circuit. In Proceedings of the **2008 Symposium on VLSI Technology and Circuits**, Hilton Hawaiian Village, Honolulu, Hawaii, June 2008.
6. Xuan-Tu Tran, Yvain Thonnart, Jean Durupt, Vincent Beroulle, and Chantal Robach. A Design-for-Test Implementation of an Asynchronous Network-on-Chip Architecture and its Associated Test Pattern Generation and Application. In Proceedings of the **ACM/IEEE International Symposium on Networks-on-Chips (NOCS 2008)**, pp. 149–158, Newcastle upon Tyne, UK, April 2008.
7. Xuan-Tu Tran. Test Method and Design-for-Test of Asynchronous Networks-on-Chip: Application to ANOC Network. **PhD thesis**, February 2008.
8. E. Beigne, P. Vivet, F. Clermidy, Y. Thonnart, A. Valentian, S. Miermont, H. Lhermet, T. Tran-Xuan, J. Durupt, D. Varreau, C. Bour. ALPIN: an Asynchronous Low-Power Innovative NoC. Demonstration at the 14th **IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC 2008)**.
9. Xuan-Tu Tran, Yvain Thonnart, Jean Durupt, F. Bertrand, Vincent Beroulle, and Chantal Robach. Implementation of a Design-for-Test Architecture for Asynchronous Networks-on-Chip. In Proceedings of the **ACM/IEEE International Symposium on Networks-on-Chips (NOCS 2007)**, pp. 216–216, New Jersey, USA, May 2007.
10. Xuan-Tu Tran, Jean Durupt, F. Bertrand, Vincent Beroulle, and Chantal Robach. How to Implement an Asynchronous Test Wrapper for Networks-on-Chip Nodes. In Informal Proceedings of the 12th **IEEE European Test Symposium (ETS 2007)**, pp. 29–34, Freiburg, Germany, May 2007.
11. Xuan-Tu Tran, Jean Durupt, F. Bertrand, Vincent Beroulle, and Chantal Robach. A DFT Architecture for Asynchronous Networks-on-Chip. In Proceedings of the **IEEE European Test Symposium (ETS 2006)**, pp. 219–224, Southampton, UK, May 2006.
12. Xuan-Tu Tran, Jean Durupt, F. Bertrand, Vincent Beroulle, and Chantal Robach. Conception en Vue de Test pour l'Architecture d'un Réseau sur Puce Asynchrone. In Proceedings of **Journées Nationa-**

les du Réseau Doctoral en Microélectronique (JNRDM 2006), pp. 504–507, Rennes, France, May 2006.

13. Xuan-Tu Tran, Vincent Beroulle, Jean Durupt, Chantal Robach, and F. Bertrand. Design-for-Test of Asynchronous Networks-on-Chip. In Proceedings of the **IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems (DDECS 2006)**, pp. 163–167, Prague, Czech, April 2006.
14. Dien-Tap Ngo and Xuan-Tu Tran. Control over the Power Lines. In Proceedings of the **Asian International Conference on Power System Protection**, pp. 578–581, Nanjing, China, October 2003.
15. Dien-Tap Ngo and Xuan-Tu Tran. Measure Temperature over the Power Lines. In Proceedings of the **8th National Conference on Radio and Electronics (REV 2002)**, pp. 377–380, Hanoi, Vietnam, November 2002.